Electronic Version
Stylesheet Version v1.1.1

MEMORY DEVICE WITH PROGRAMMABLE RECEIVERS TO IMPROVE PERFORMANCE

Abstract

A memory system having a plurality of DRAMs which are selectively provided non-inverted or inverted signals. The DRAMs have the ability to accept non-inverted or inverted address/command signals from a register that drives a plurality of signals simultaneously. The system includes DRAM receivers with programmable input polarity and a register with programmable output polarity.